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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/828,573	04/02/2001	Ramesh Duvvuru	388682000700	6602

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EXAMINER	
CASIANO, ANGEL L	
ART UNIT	**PAPER NUMBER**
2182	

DATE MAILED: 10/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/828,573	DUVVURU, RAMESH
	Examiner	Art Unit
	Angel L Casiano	2182

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,7-9 and 13-15* is/are rejected.

7)☒ Claim(s) *4-6,10-12 and 16-18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment

The present Office action is in response to Amendment dated 21 June 2004.

Claims 1-18 are pending in the application.

Drawings

1. Previous Objections to the Drawings have been overcome with the corrections included in the present Amendment.

Claim Rejections - 35 USC § 112

2. Previous Rejections under 35 USC 112, 2nd paragraph have been overcome with the modifications (claim 1) included in the present Amendment.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

   (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3, 7-9 and 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hadziomerovic [EP 0147086] in view of Bagheri et al., "10 Gb/s Framer/Demultiplexer IC for SONET STS-192 Applications", 1995 IEEE.

Regarding claim 1, Hadziomerovic teaches an apparatus for processing bytes received from a data stream (see Abstract). The cited reference teaches receiving data (bytes) from a data channel during clock cycles (see page 2, lines 22-35). Hadziomerovic also teaches an apparatus capable of generating data regarding the status of the bytes (see page 8, line 11; page 23, lines 3-29). Hadziomerovic clearly teaches the indication of a flag byte (see Abstract; Figure 1, "10", "20"). The Hadziomerovic reference also discloses using flags for designating delineating bytes (see page 1, line 21; Figure 1; page 2, lines 1-5). Nonetheless, Hadziomerovic teaches serial, instead of parallel processing, as claimed. In addition, the cited art does not explicitly teach an "input formatter" as recited by the claim. Regarding these limitations, Bagheri teaches a data stream, where serial data is converted into "a byte-parallel, frame-synchronized output data stream" (see Abstract, page 427). Therefore, the Bagheri reference teaches parallel processing. At the time of the invention, one of ordinary skill in the would have been motivated to apply parallel processing and communication, as disclosed by Bagheri et al., since the disclosure teaches bandwidth optimization (see Introduction, page 427) in a SONET (Synchronous Optical Network) environment as well as integrating multiple functions (serial to parallel conversion, byte alignment, and frame detection).

As for claim 2, Hadziomerovic teaches a status register (see page 8, lines 11-20). In addition, the reference also teaches using flags for designating delineating bytes (see page 1, line 21; Figure 1; page 2, lines 1-5).

As for claim 3, Hadziomerovic discloses status registers (see page 8, lines 11-12). The cited art also uses flags for designating delineating bytes (see page 1, line 21; Figure 1; page 2, lines 1-5). The cited disclosure includes delineation for the frames (see HDLC, Figure 1).

Regarding claim 7, Hadziomerovic exposes an apparatus for processing bytes received from a data stream (see Abstract). The cited art teaches receiving data (bytes) from a data channel during a cycle (see page 2, lines 22-35). Hadziomerovic also teaches an apparatus capable of generating byte status data (see page 8, line 11; page 23, lines 3-29). Hadziomerovic clearly teaches the indication of a flag byte (see Abstract; Figure 1, "10", "20"). The cited art also discloses using flags for designating delineating bytes (see page 1, line 21; Figure 1; page 2, lines 1-5). Nonetheless, Hadziomerovic teaches serial, instead of parallel processing (as claimed). In addition, the cited art does not explicitly teach "input formatter means" as recited in the claim. Regarding these limitations, Bagheri teaches a data stream, where serial data is converted into "a byte-parallel, frame-synchronized output data stream" (see Abstract, page 427). Therefore, the Bagheri reference teaches parallel processing. At the time of the invention, one of ordinary skill in the would have been motivated to apply parallel processing and communication, as disclosed by Bagheri et al., since the disclosure teaches bandwidth optimization (see Introduction, page

427) in a SONET (Synchronous Optical Network) environment as well as integrating multiple functions (serial to parallel conversion, byte alignment, and frame detection).

As per claim 8, Hadziomerovic teaches status register means (see page 8, lines 11-20). In addition, the reference teaches using flags for designating delineating bytes (see page 1, line 21; Figure 1; page 2, lines 1-5).

As for claim 9, Hadziomerovic exposes status register means (see page 8, lines 11-12). The cited art also uses flags for designating delineating bytes (see page 1, line 21; Figure 1; page 2, lines 1-5). The cited disclosure includes delineation for the frames (see HDLC, Figure 1).

Regarding claims 13-15, these constitute the method of processing bytes received from a data stream. The claimed method includes the steps of "receiving", "generating", and "processing". The combination of prior art cited in the present Office action teaches or suggests the limitations corresponding to the apparatus (see Rejections above) and therefore, the method. Accordingly, these claims are rejected under the same rationale.

Allowable Subject Matter

5. Claims 4-6, 10-12, and 16-18 were previously objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

6. Applicant's arguments filed 21 June 2004 have been fully considered but they are not persuasive. Examiner respectfully maintains his position as stated in previous Office action.

7. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., Page 13; "SONET frame" and "two separate stages of byte processing (1) and (2)") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Examiner has considered all the arguments presented by the Applicant. However, in reference to claim 1 in particular, these seem to be more specific than the claim language. For example, Applicant (Page 14 of the Remarks) argues that "a novel aspect of the present invention lies in the processing of data stream bytes in parallel and communicating byte status information to *other* byte processing *engines* during the *same* processing *cycle*" (emphasis added). In claim 1, "parallel byte processing engines" receive bytes from a "data channel" and generate "byte status data". Then, an "*input formatter*" receives the "status data" from the "parallel byte processing engines" (emphasis added).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

- Maa [US 5,878,057] teaches highly parallel cyclic redundancy code generator.

- Upp et al. [US 5,040,170] teaches processing data in byte-parallel format; SONET format.

9. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Angel L Casiano whose telephone number is 571-272-4142. The examiner can normally be reached on 9:00-5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey Gaffin can be reached on 571-272-4146. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alc
29 September 2004.

JEFFREY GAFFIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100